Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action in the above-identified patent application. Claims 7, 11, 24 and 25 are allowed. Claims 38-47 have been amended to expedite prosecution.

Claims 42-43 and 46-47 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claims 39-43 and 45-47 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 38 and 40-47 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dietl et al.* (U.S. Patent No. 6,556,088).

Claims 38 and 39 are rejected under 35 U.S.C. §102(b) as being anticipated by *Maneatis* (U.S. Patent No. 5,727,037).

I. Rejection of Claims 42-43 and 46-47 under 35 U.S.C. §112, First Paragraph

Claims 42-43 and 46-47 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

The Office Action's Response to Applicant's Arguments states:

> Examiner respectfully disagrees [that fig. 1a-b and its description at least satisfies the written description requirement] since component 102, 103, 112 and 113 has a single current input then it cannot be a clock buffer, let alone a phase mixer. Office Action, pages 5-6.

However, the instant Specification states:

> Bias current I_{bias}, which is proportional to current I_{ld}, is provided to circuit components of the PLL/DLL, such as a charge pump, phase mixer, amplifier, clock buffer and loop resistor, from an interconnect in embodiments of the present invention…Figs. 1a and 1b **illustrate portions of a PLL and DLL**, respectively. In particular, current I_{ld} is input to VCO 100 and VCDL 110, while copies of current I_{ld} are provided to circuit components 102 and 103, and circuit components 112 and 113, respectively. In an embodiment of the present invention, a circuit component of the PLL/DLL includes a bias-generating device, such as a MOSFET p-type transistor having a drain coupled to the interconnect. (Emphasis Added.) Page 3, lines 14-23.

Contrary to the Office Action's assertions, Figs. 1a and 1b illustrate "portions of a PLL and DLL" and thus not every input and output is illustrated. Figs. 1a and 1b are provided to illustrate at least the

distribution of current I_{id} to circuit components, such as a phase mixer or clock buffer. In a particular embodiment, the instant Specification describes that current I_{id} (or current I_{bias} in alternate embodiments, see Specification page 4, lines 14-16) is distributed by way of an interconnect to "a circuit component of the PLL/DLL that includes a bias-generating device, such as a MOSFET p-type transistor having a drain coupled to the interconnect."

Also, the Specification explicitly states: "In an alternate embodiment of the present invention, interconnections shown as a single signal line in the Figures represent multiple signal lines or a bus." (Emphasis added.) Specification page 5, lines 4-6. Thus, the single signal line (or interconnect) in Figs 1a and 1b may represent multiple signal lines in alternate embodiments.

The Office Action's Response to Applicant's Arguments further states:

> There is no description of phase mixer or clock buffer on page 3 of the specification. Terms "phase mixer" and "clock buffer" are mentioned on page 3 without descriptions pertaining to their structure and/or operation aspects with the inventive apparatus. Office Action, page 6.

The Applicant's attorney respectfully disagrees.

First, as seen above, the Specification does describe "the structure and/or operation aspects" of the phase mixer and/or clock buffer. In particular, the specification describes a phase mixer and/or clock buffer embodiment that "includes a bias-generating device, such as a MOSFET p-type transistor having a drain coupled to the interconnect." The Specification also describes the properties or equations (5)-(8) associated with current I_{id} and the MOSFET device that is included in a circuit component, such as a phase mixer and/or clock buffer, at least at page 10, lines 1-16.

Second, "Section 112 does not require that the specification contain that which is known to those skilled in the art." *Martin V. Mayer*, 823 F.2d 500 at 505, 3 USPQ2d 1333 at 1337 (Fed. Cir. 1987). One of ordinary skill in the art knows the structure of a typical "phase mixer" and "clock buffer" and the Applicant does not have to describe what is known by one of ordinary skill in art.

Third, "[t]he test for compliance with §112 has always required sufficient information in the original disclosure to show that the inventor possessed the invention at the time of the original filing..."*Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1320, 66 USPQ2d 1429 (Fed. Cir. 2003), *cert denied*, 540 U.S. 982 (2003). The inventor describes in written detail the differences and problems overcome by current biasing circuit components of a PLL/DLL as opposed to voltage biasing. Specification pages 1-2, 8-11. The inventor described/derived the equations and properties associated with current I_{id} and a bias generating MOSFET device. The inventor also describes a specific example of using "a bias-generating device 605"

along with at least eight other transistors in a circuit component. Page 10-11, Fig. 6. The inventor clearly provided sufficient information to show possession of the claimed invention.

It is therefore respectfully requested that the rejection of claims 42-43 and 46-47 under 35 U.S.C. §112, first paragraph, be withdrawn.

II. Rejection of Claims 39-43 and 45-47 under 35 U.S.C. §112, Second Paragraph

Claims 39-43 and 45-47 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Office Action's Response to Applicant's Arguments states:

> Applicant is reminded that lines 27+ of page 11 disclose bias current Ibias derived from current Iid. And independent claims clearly recite "the voltage regulator provides a first bias current to the charge pump based on the load current." Further, charge pump and voltage regulator are two distinct entities. Therefore, it is incorrect to recite "charge pump…to output the first bias current." Office Action, page 6.

The Examiner is respectfully reminded that "lines 27+ of page 11" describe at least one embodiment; yet, the Specification describes may other embodiments as well. For example, "bias current circuit network 208 (shown as dashed lines) provides a bias current I_{bias} to circuit components of DLL 200 which is proportional to current I_{ld}. In an embodiment of the present invention, bias circuit network 208 is a series of current mirrors." Specification, pages 5-6, lines 27-29 and 1-2.

Nevertheless, claims 38-47 have been amended to expedite prosecution.

It is therefore respectfully requested that the rejection of claims 39-43 and 45-47 under 35 U.S.C. §112, second paragraph, be withdrawn.

III. Rejection of Claims 38 and 40-47 under 35 U.S.C. §102(e)

Claims 38 and 40-47 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dietl et al.*

The Office Action's Response to Applicant's Arguments states:

> It is noted that "load current" and "a first bias current" can be the same since the recitation of the claim does not make a distinction between the above two currents. Further, figure 2 of the instant application shows the same current provided to VCO and charge pump on different traces. Lastly, load current and bias current are considered the same since one is mirrored from the other as shown in figure 6. Office Action, page 6.

The Examiner is improperly ignoring two distinctly claimed elements. Independent claims 38 and 44 claim two distinct currents: "a load current" and "a bias current." The Examiner previously admits in the present Office Action that the Specification discloses an embodiment using two separate currents: "Applicant is reminded that lines 27+ of page 11 disclose bias current Ibias is derived from current Iid." (Emphasis added.) Office Action page 6, line 6. However, the Examiner now contradicts this admission by stating the "load current" and "a first bias current" are the same.

Furthermore, the instant Specification clearly discloses an embodiment that includes two distinct currents:

> A copy of current I_{id} provided to a VCO 106 is input to bias current circuit network 108 that provides a proportional bias current I_{bias} to bias-generating devices in a circuit component of PLL 100. Specification, page 3, lines 14-17.

The Office Action's Response to Applicant's Arguments further states in regard to claim 44: "There is no different [sic, difference] in scopes [sic, scope] of claims 38 and 40." Office Action, page 6.

The Applicant's attorney respectfully disagrees. Claims 38 and 44 have distinctly different claim elements. Claim 38 calls for "a voltage-controlled oscillator" while claim 44 calls for "a voltage-controlled delay line" that the Examiner has not identified as being disclosed in *Dietl et al.* (Emphasis added.)

Claims 45-47 depend from claim 44 and therefore are patentable for the reasons stated above in regard to claim 44.

The Office Action's Response to Applicant's Arguments further states:

> Claims 45-47 are seen as "intended use" since they merely receive an input from the claimed apparatus of independent clam for their own operation. The very existing, or lacking, of components recited in claim 45-47 will not change functional/operational characteristics of the claimed invention in the dependent claims. Office Action, page 6-7.

The Applicant's attorney respectfully disagrees that claims 45-47 merely claim an "intended use." Claims 45-47 clearly claim structure, such as at least: "a semiconductor device," "a phase mixer" and "a clock buffer" and not an intended use.

Further, the Examiner has not identified in *Dietl et al.* "a phase mixer…" and "a clock buffer…" as required by claims 46 and 47.

It is therefore respectfully requested that the rejection of claims 38 and 40-47 under 35 U.S.C. §102(e) be withdrawn.

IV. Rejection of Claims 38 and 39 under 35 U.S.C. §102(b)

Claims 38 and 39 are rejected under 35 U.S.C. §102(b) as being anticipated by *Maneatis*.

The Office Action's Response to Applicant's Arguments states:

> Examiner respectfully disagrees since "a first bias current" and "load current" are seen as the same since there is no clear distinction as recited in claim and drawings do not show them distinctly different. Office Action, page 7.

The Applicant's attorney respectfully disagrees for similar reasons, stated above, regarding the rejections based on *Dietl et al.*

Further, the Examiner's reasoning for the rejection based on the "drawings" allegedly "not show[ing] them distinctly different" is not a proper reasoning under a 35 U.S.C. §102(b) rejection. The Examiner should identify all the specific claim limitations in a single prior art reference and not what is or is not shown in the instant Drawing.

It is therefore respectfully requested that the rejection of claims 38 and 39 under 35 U.S.C. §102(b) be withdrawn.

V. Conclusion

Based on the above amendments and these remarks, reconsideration of the presently pending claims is respectfully requested.

Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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